REMARKS

New Claims 7-10 are pending in the application, with claims 1-6 cancelled by this amendment. No new matter is added by these amendments.

A substitute Abstract is included herewith. As to the specified objections, applicant's attorneys respond as follows:

As to the "serial signal for testing purposes" this term has been amended to recite "a serial testing signal." Thus, Applicants have adopted the Examiner's suggestion for clarification.

As to the "measured devices" the Examiner has with the ability of one skilled in the art determined exactly what this term means, it refers to the devices under test (Office Action Page 4). Thus it is unclear how this term can be undefined. Indeed, though no specific definition is provided, through reference to the drawings and the specification, it is clear that the Applicant has provided adequate explanation as to the meaning of this term.

Next, as to "a passing signal passing through the redundant channel," this phrase has been amended to recite "one of the plurality of parallel signals being a passing signal passing through the redundant channel." It is believed that this clarifies that one of the parallel signals passes through a redundant channel, which the specification defines as for example channel 16 in Fig. 5.

Finally, with respect to the phrase "bit errors are measured in the multiplexed signals and measured devices at which the bit errors are generated are detected in consideration of the channel determination signal," those of skill in the art will readily appreciate that this simply means that the channel determination is used as a reference for measuring bit errors and detecting which of the measured devices are generating the bit errors. Thus, it is

submitted that this phrase is suitably clear to allow one of skill in the art to understand its meaning.

In view of the foregoing amendments and remarks considering the abstract, it is requested that the objections thereto be withdrawn.

Next, the office action rejects the specification under 35 U.S.C. § 112, first paragraph as failing to be written "in such full, clear, concise, and exact terms as to enable any person in the art to which it pertains...to make and use the same." It is submitted that the specification, as written meets this standard.

As discussed above, the term "measured devices" is used throughout the specification and the drawings. By such use the Applicant has provided sufficient definition to allow one of skill in the art to understand its meaning, as is evident by the Examiner's proper understanding of the term.

Further, as to the "measuring occurrence of bit errors are measured in the multiplexed signals and measured devices at which the bit errors are generated are detected in consideration of the channel determination signal," though perhaps inartfully worded, nonetheless is of sufficient clarity to understand the meaning of the terms as discussed above.

The Examiner has previously requested a substitute specification, an arduous and expensive proposition for any applicant, but one which was nonetheless complied with. To request a second substitute specification, when the meaning of the terms is more than sufficiently explained in the specification to meet the standard of § 112 is unnecessary and the Examiner's is requested to withdraw the request.

Next, the Office Action references page 5 of the substitute specification, as failing to meet the standards of § 112, first paragraph. After review of these alleged offending sections,

the undersigned attorney can only find one paragraph, that beginning on line 21 which inadvertently included the statement "measured in the parallel in a parallel measurement system." This language has been amended, as shown above, to remove the phrase "in a parallel" and remove the unclear statement.

Finally, with respect to the clarity of the specification, it is submitted that the requirements of § 112 do not require that the specification be written in the manner in which the Examiner would prefer, or in the manner the Examiner would write it, but rather in a manner that enables one skilled in the art to make and use the invention, as stated repeatedly herein, it is believed that in its current form, the specification meets this requirement.

Accordingly withdrawal of the rejections under § 112, first paragraph is respectfully requested.

Claims 1-6 are rejected under 37 C.F.R. § 112, second paragraph. It is submitted that as claims 1-6 have been cancelled, and the new claims do not included the alleged offending language, this rejection is now moot.

On the merits, the office action claims 1 and 4 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,566,193 to Cloonan. As these claims are cancelled, it is submitted that this rejection is now moot. However, to further prosecution, this rejection will be addressed in comparison to the new claims.

One aspect of the present invention, as claimed, is directed to detecting bit errors. To do this a serial signal is de-multiplexed into several signals, which are transmitted through the devices being analyzed. The output of these devices is then multiplexed. One of these parallel signals is not sent through a device but sent to the multiplexer through an all bit error generating circuit 6, as shown in Fig. 5.

As the signal is de-multiplexed it may have, as shown in Fig. 3, channels 1-9, and 0. During transmission, the order of these channels does not change, however, because the start time of the error detection varies, there must be a way to determine which of the channels corresponds to the channel where the detection has started. In Fig. 3, for example, the detection begins with channel 4.

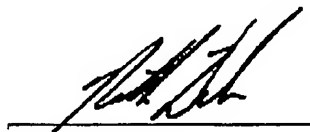
As shown in Figs. 2 and 3, Ch 10 is (0) and all of the bits of Ch. 10 are, for example inverted to create a 100% error rate. This is achieved by the "All bit Error Generating Circuit" 6 or "channel marking device." Typically, such an error rate is not achieved in a transmission line. As a result this error rate is used to identify Ch. 10, thus this signal can be used to distinguish Ch 10, that is signal 0, from the other signals. See Fig. 3, there is a black bar to 100% for the 7^{th} channel measured, which corresponds to Ch10 or (0) as the actual channel. By comparing the location of the Ch. 10 (0), the actual error bits or devices causing errors can be determined regardless of the timing of the testing onset.

In the instant claims, the use of the Ch 10 or Ch (N) and creating a signal with a 100% error rate is performed by a "channel marking device" as recited in new claims 7 and 9. Such a feature is not described in the relied upon portions of Cloonan cited by the Examiner. Accordingly, it is submitted that claims 7 and 9 patentably distinguish over the relied upon portions of the cited reference and are allowable. Claims 8 and 10 depend from these allowable base claims and are allowable therewith.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



Nathan Weber
Reg. No. 50,958

CUSTOMER NUMBER 026304
Telephone: (212) 940-8564
Fax: (212) 940-8986 or 8987
Docket No.: FUJZ 20.674 (100794-00486)
NDW: